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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,154	07/30/2003	Yi Ding	M-15230 US	1878

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,154	YI DING	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *18-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *042004* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-17, drawn to a method of fabricating an integrated circuit comprising a nonvolatile memory, classified in class 438, subclass 257.

   II. Claims 18-29, drawn to an integrated circuit, classified in class 257, subclass 296.

2. The inventions are distinct, each from the other because of the following reasons: Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process such as one in which the process of fabricating an integrated circuit having the floating gates and the control gates formed for the memory cell before the select gate is formed instead.

   Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

   During a telephone conversation with attorney Michael Shenker on 07/12/2004 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-17. Affirmation of this election must be made by applicant in replying to this Office action. Claims 18-29 withdrawn from further

consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Yaegashi et al. (U.S. Patent 6,265,739).

In re claim 1, **Yaegashi** discloses a method for fabricating an integrated circuit comprising a nonvolatile memory comprising a nonvolatile memory cell comprising two floating gates (**FIG. 4A: 106**, in MEMORY CELL region), a select gate (inside the SELECT TRANSISTOR), and two control gates (**FIG. 4A: 107**, in MEMORY CELL region), the nonvolatile memory further comprising a

first peripheral transistor **(FIG. 4A: Vpp-Tr)**, the method comprising: (a) forming a dielectric layer on a semiconductor substrate **(FIG. 4A: 101)**, the dielectric layer comprising a first dielectric region **(FIG. 4A: 108)** ("select gate dielectric'') and a second dielectric region **(FIG. 4A: 108**, inside Vpp-Tr) ("first peripheral transistor gate dielectric'') (col. 7, line 57 to col. 8, line 29), wherein the select gate dielectric and the first peripheral transistor gate dielectric are formed simultaneously (col. 9, lines 53-61); (b) forming a first layer over the dielectric layer and patterning the first layer to provide (i) the select gate on the select gate dielectric **(FIG. 4A: SELECT TRANSISTOR)**, and (ii) a gate for the first peripheral transistor on the first peripheral transistor gate dielectric **(FIG. 4A: Vpp-Tr)** (col. 8, lines 41-54); (c) after the operation (b), forming the floating gates **(FIG. 4A: 106, in MEMORY CELL region)** and the control gates **(FIG. 4A: 106, in MEMORY CELL region)** for the memory cell **(FIGS. 1-4B)**.

In re claim 2, **Yaegashi** discloses wherein the memory cell comprises a channel region in the semiconductor substrate **101**, the select gate controls a conductivity of a portion of the channel region, and each of the floating gates **106** overlies a respective other portion of the channel region (col. 10, lines 16-65 and **FIGS. 4A-6C**).

In re claim 3, **Yaegashi** discloses wherein the control gates **107** overlie the respective floating gates **106 (FIG. 4A)**.

In re claim 4, **Yaegashi** discloses wherein the operation (b) comprises forming a plurality of layers (**106** and **107**) over the semiconductor substrate **101**

(FIGS. 2A-C), wherein the floating gates **106** and the control gates **107** are formed from the plurality of layers **(FIG. 4A)**.

In re claim 5, **Yaegashi** discloses wherein the select gate dielectric **108** and the first peripheral transistor gate dielectric **108** (in Vpp-Tr region) are formed by oxidation of the semiconductor substrate **101** (FIG. 4A) (col. 9, lines 32-34).

In re claim 6, **Yaegashi** discloses wherein the select gate dielectric **108** and the first peripheral transistor gate dielectric **108** (in Vpp-Tr region) comprise silicon oxide (col. 9, lines 22-34).

In re claim 7, **Yaegashi** discloses wherein the method of Claim 1 further comprising, after the operation (b), forming a dielectric **105** ("floating gate dielectric") on the semiconductor substrate **101** to separate the floating gates **106** from the substrate, wherein the floating gate dielectric (8nm thick) is formed of the same material as the select gate dielectric **108** (40 nm thick) (col. 9, lines 53-61) but is thinner than the select gate dielectric (col. 8, lines 30-39 and **FIG. 4A**).

In re claim 8, **Yaegashi** discloses wherein the method of Claim 1 further comprising forming a second peripheral transistor gate dielectric **118** (Vcc-Tr) on the semiconductor substrate **101** for a second peripheral transistor (Vcc-Tr), and forming a gate **106, 107** of the second peripheral transistor on the second peripheral transistor gate dielectric, wherein the second peripheral transistor gate dielectric **118** is made from the same material as the select gate dielectric **108** (SELECT TRANSISTOR) and the first peripheral transistor gate dielectric **108** (Vpp-Tr) but the thickness of the second peripheral transistor gate dielectric (8 nm

thick) is different from the thickness of the first peripheral transistor gate dielectric (40 nm) (col. 9, lines 53-61 and **FIG. 4A**).

In re claim 9, **Yaegashi** discloses wherein the second peripheral transistor gate dielectric **118** (Vcc-Tr) (8nm thick) is thinner than the first peripheral transistor gate dielectric **108** (Vpp-Tr) (40nm thick) (col. 9, lines 53-61 and **FIG. 4A**).

In re claim 10, **Yaegashi** discloses wherein the select gate dielectric as at least as thick as a gate dielectric of any peripheral transistor in the memory (col. 9, lines 53-61 and **FIG. 4A**).

In re claim 11, **Yaegashi** discloses wherein the second peripheral transistor gate dielectric is formed after the start of the operation (a) (col. 9, lines 16-61 and **FIGS. 1-4A**).

In re claim 12, **Yaegashi** discloses wherein the second peripheral transistor gate dielectric **118** (Vcc-Tr) is formed before the operation (b) (col. 9, lines 53-61 and FIGS. 1-4A).

In re claim 13, **Yaegashi** discloses wherein the gate **106** and **107** of the second peripheral transistor (Vcc-Tr) is formed by patterning the first layer in the operation (b) (col. 8, lines 5-54 and **FIGS. 1-4A**).

In re claim 14, **Yaegashi** discloses wherein the memory cell is one of a plurality of nonvolatile memory cells of the memory, each memory cell comprising two floating gates **106**, a select gate (in SELECT TRANSISSTOR), and two control gates **107**, wherein: the operation (a) simultaneously forms select gate dielectric for each of the memory cells; and the operation (b) simultaneously

forms the select gate for each of the memory cells on the corresponding select gate dielectric (col. 8, lines 5-54 and **FIGS. 1-4A**).

In re claim 15, **Yaegashi** discloses wherein during a memory cell writing operation, the first peripheral transistor (Vpp Tr) is exposed to a voltage of a higher magnitude than any voltage provided to the memory cell in a reading operation (col. 7, line 57 to col. 8, line 4 and **FIGS. 1-4A**).

In re claim 16, **Yaegashi** discloses wherein during the memory cell writing operation, the first peripheral transistor is exposed to a voltage of a higher magnitude than any power supply voltage provided to the nonvolatile memory (col. 7, line 57 to col. 8, line 4 and **FIGS. 1-4A**).

In re claim 17, **Yaegashi** discloses wherein the memory is to support a writing operation in which the memory cell is written by a transfer of a charge between one of the floating gates and a channel region of the memory cell, the channel region being located in the semiconductor substrate (col. 7, line 57 to col. 8, line 39 and **FIGS. 1-4A**).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is

assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
July 23, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER

W. DAVID COLEMAN
PRIMARY EXAMINER